

# **Progress and remaining challenges of EUV lithography for memory IC manufacturing**

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**SK hynix**

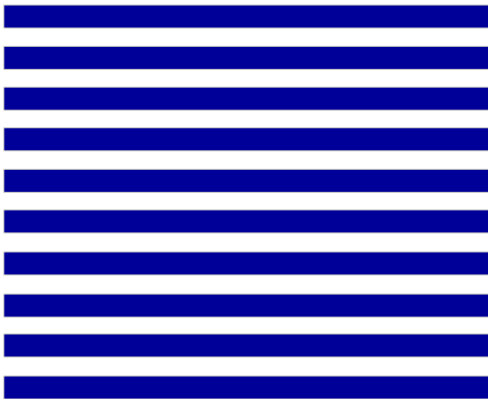
# Contents

- ✓ **Lithography for memory IC**
  - Patterning of memory IC
  - Cost and Productivity of EUV
- ✓ **Progress and challenges**
  - Source and throughput
  - Resolution and CDU
  - Overlay
  - Mask related issues
- ✓ **Closing**

# Patterning of memory IC

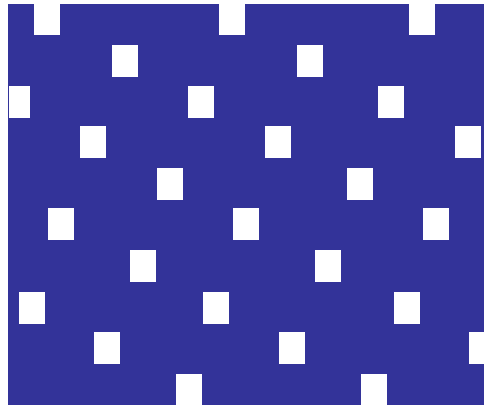
*Extremely **fine** and **dense** patterns,  
while **simple** and **repeating**!*

Lines and spaces

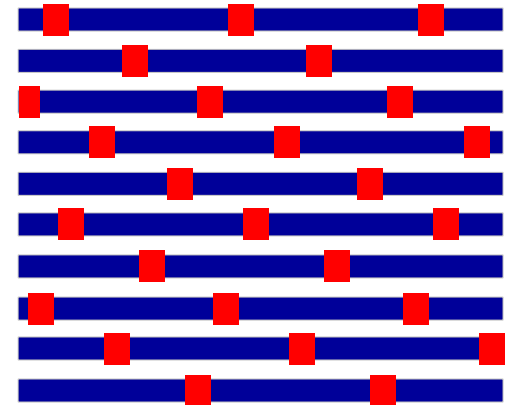


LELE, Spacer ...

Contact holes

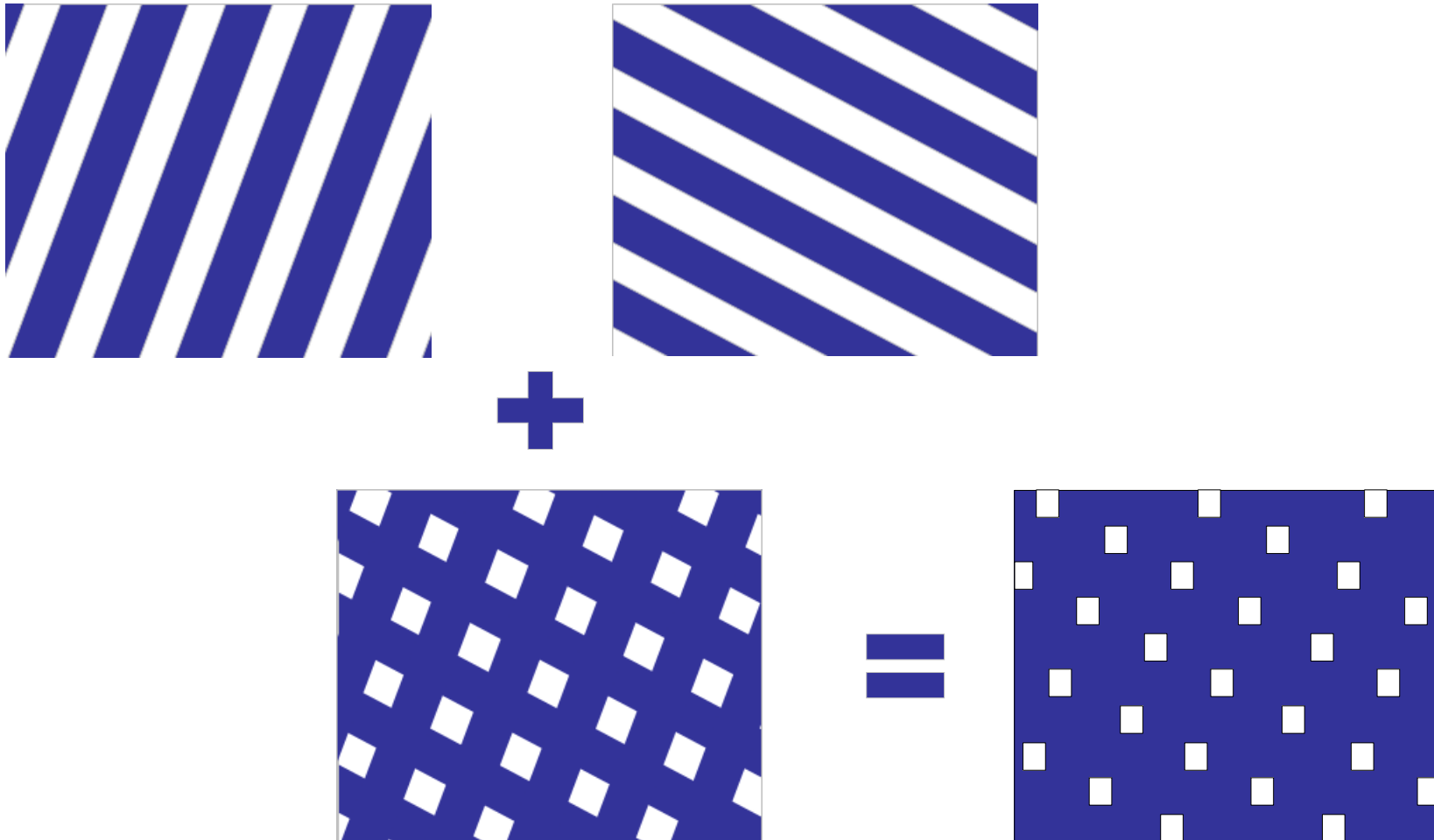


or together



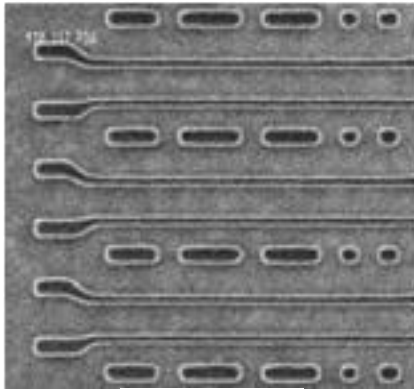
# Hole pattern by crossing lines

- sub-resolution contacts formed by multiple crossing lines

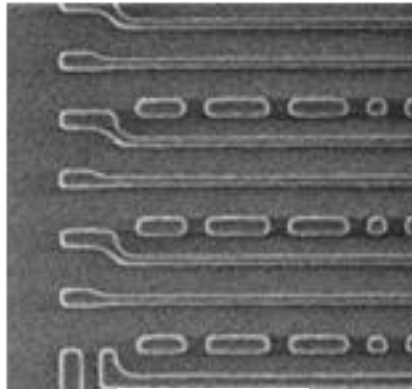


# Traditional LELE DPT

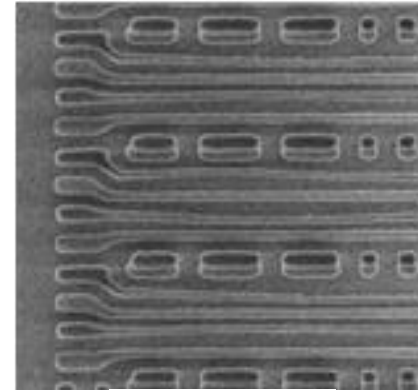
- ❑ for Complex layout in DRAM periphery



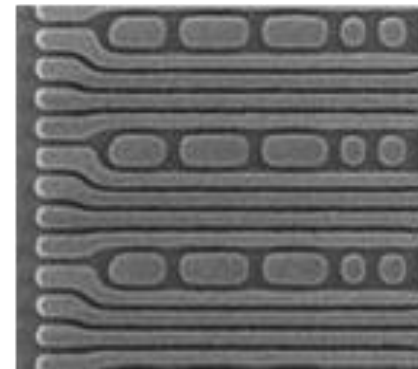
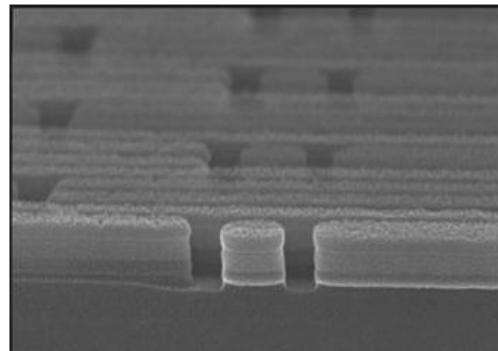
1<sup>st</sup> litho



2<sup>nd</sup> litho



Combined



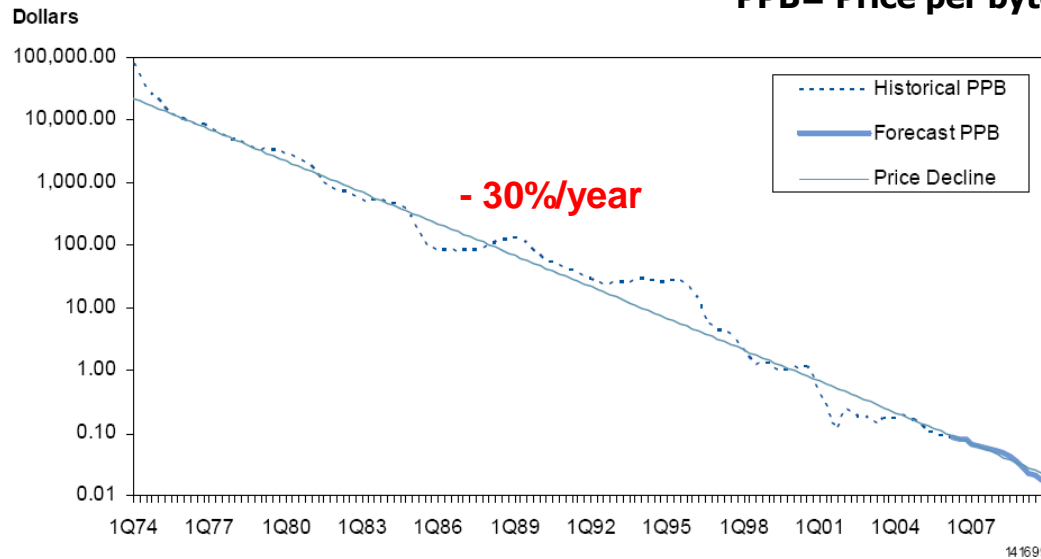
Transferred



ArF immersion capable of memory patterning whatsoever with increased process complexity

# Moore's law in Economics

PPB= Price per byte



PPM = price per byte

Source: Gartner Dataquest (November 2006)

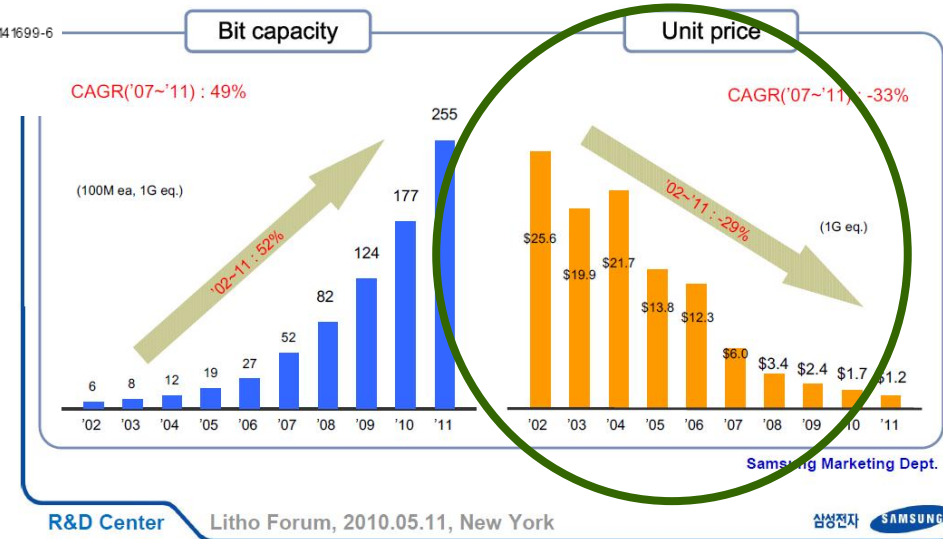
2X Bit growth every 2 years  
=Bit price -50% every 2 years

Very cost sensitive business!

## Memory Market trend

SAMSUNG DIGITAL everyone's invited.

Memory shrinkage continues!!



# Virtue of lithography for memory

*Productivity! Productivity! Productivity!*

*and*

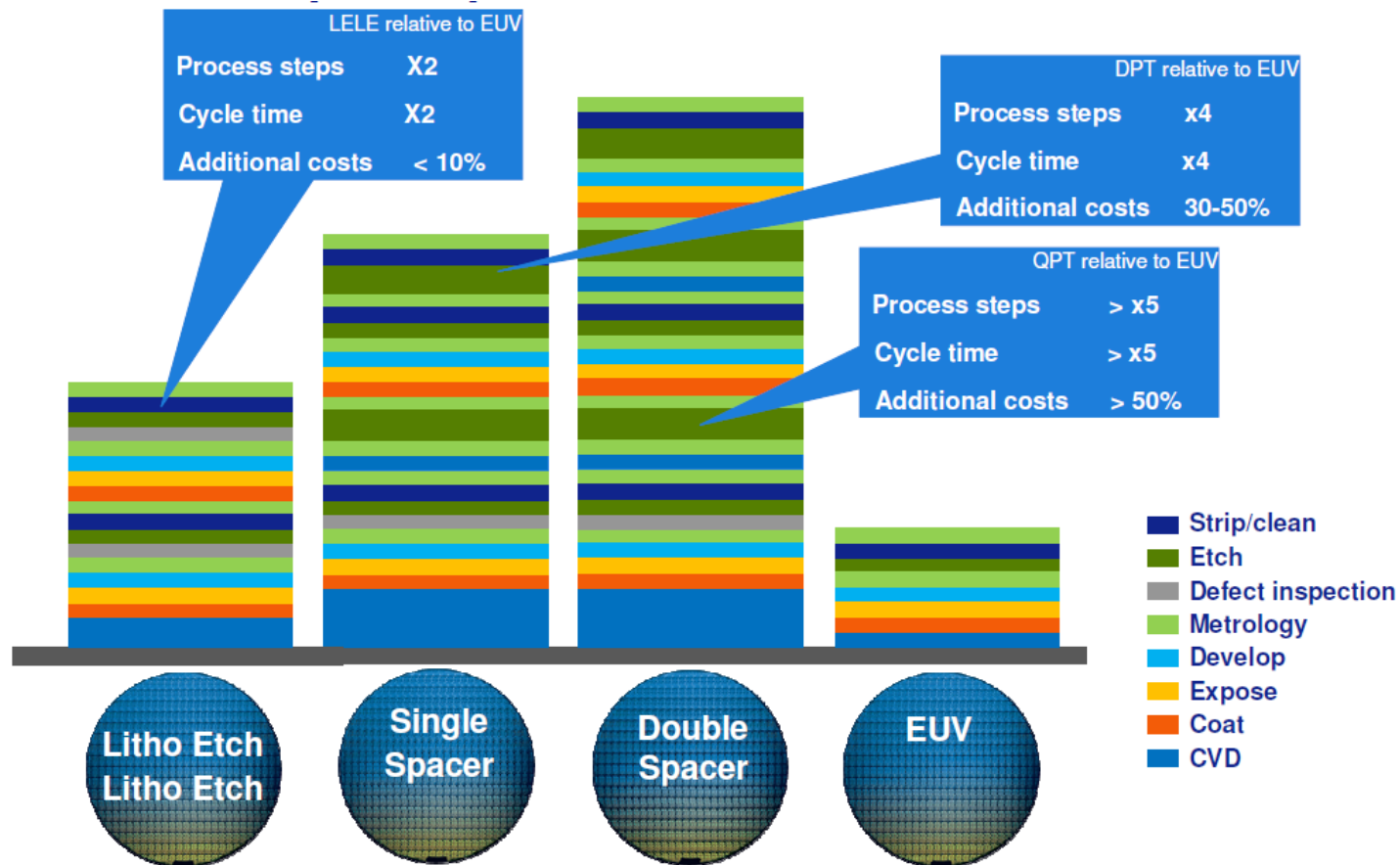
*Resolution (CD uniformity)+*

*Corresponding overlay control (~20% of D.R. or less)*

*Defect control*

# Complexity of DPT and cost

✂ Rudy Peeters(ASML) EUVL Symposium 2011



Data is based on Customer interaction

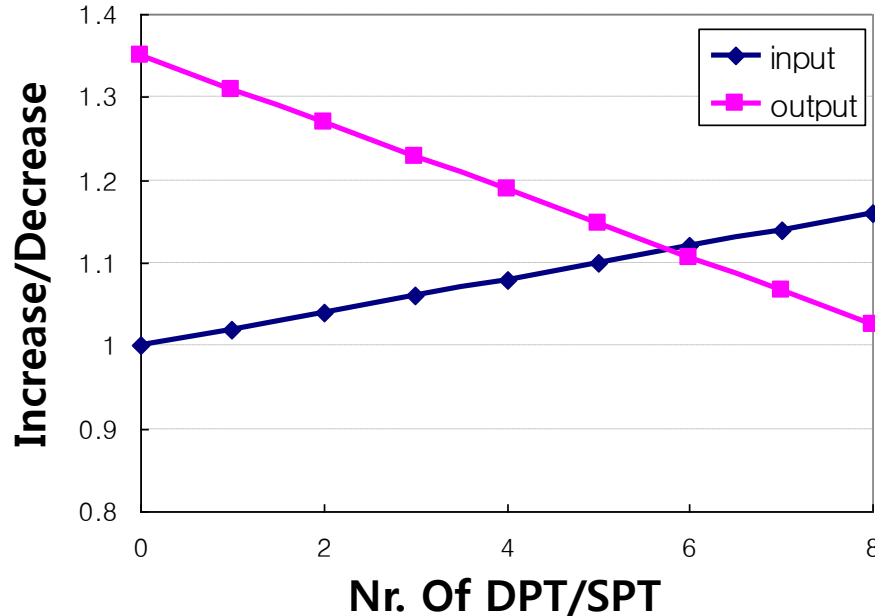
Slide 5 | Public



# Simple economics of double patterning

## □ If

- Cost increased by 1 DPT/SPT ~ 2%
- Steps increased by 1 DPT/SPT, 10~15 steps (Capa. loss~3%)
- Net die increase by shrink ~ 35%

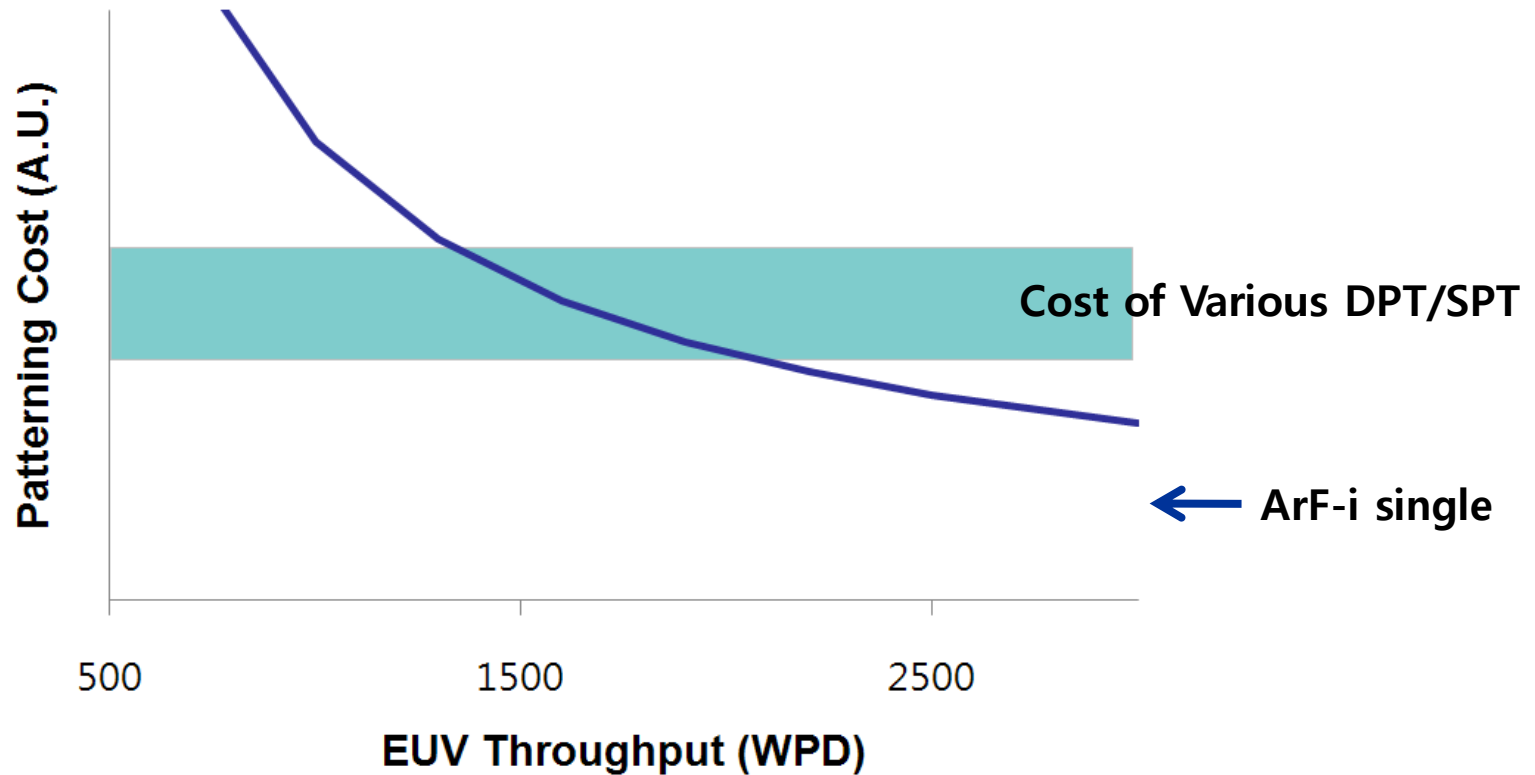


+ Yield-loss, TAT loss,  
Layout design complexity,  
Clean Room consumption

**Shrink will not help if too many D(S)PT layers are used**

# Scanner throughput is key for cost

## □ Patterning Cost vs. scanner throughput



First overcome D(S)PT, then get close to the level of ArF-I single

# Unanswered question

**Economic**  
**User-friendly**  
**Versatile**  
**Lithography**

*High  $k_1$*

*Resolution  
overlay*



**EUV**



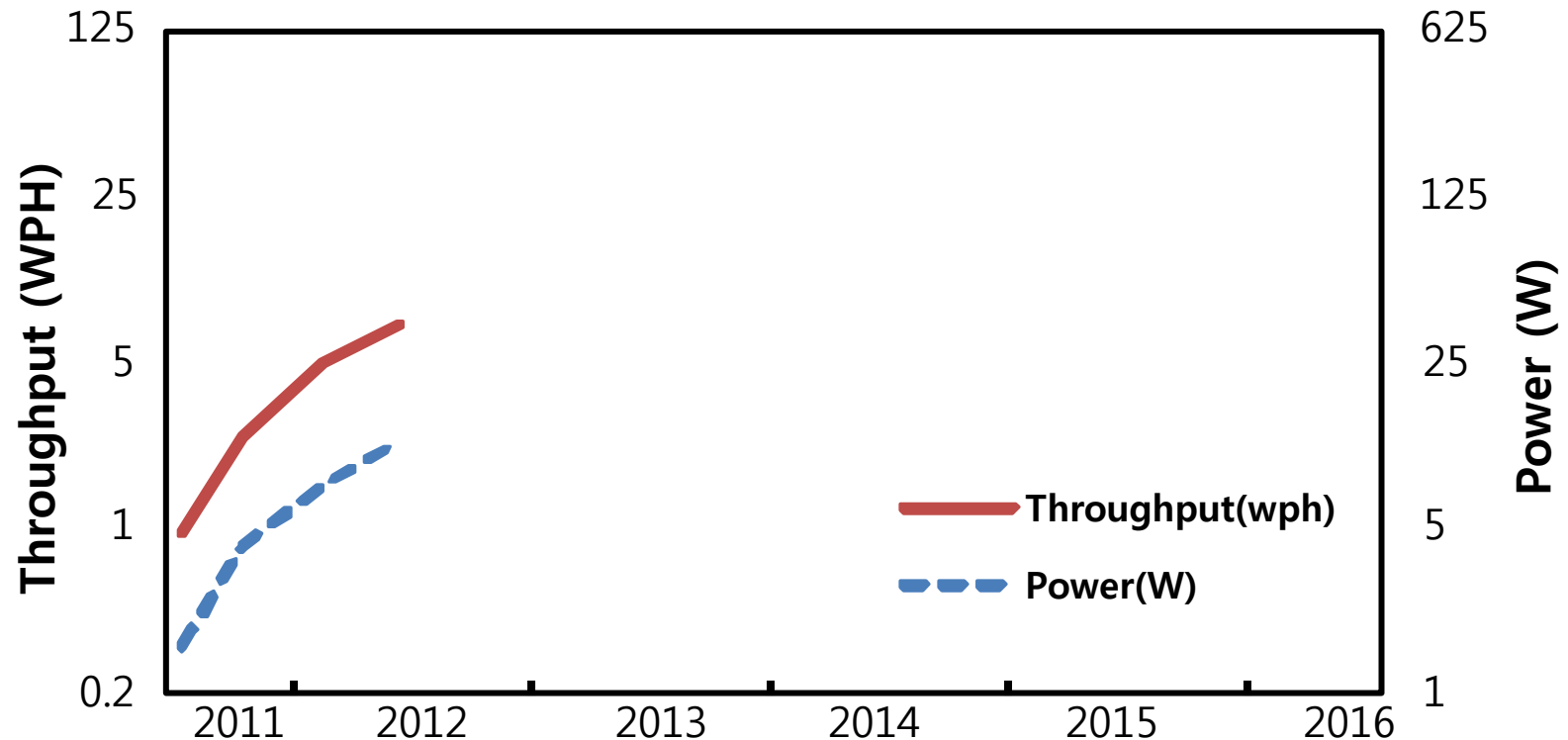
**Expensive**  
**Under-powered**  
**Vague**  
**Lithography**

*Continuous slip  
of source*

*Nobody knows*

# Real source improvement

\*Throughput : based on ASML ATP



After NXE3100 install, observed real progress, though not sufficient for HVM

# History of 248nm & 193nm

※ Hueber et. al. (Cymer) SPIE 2000

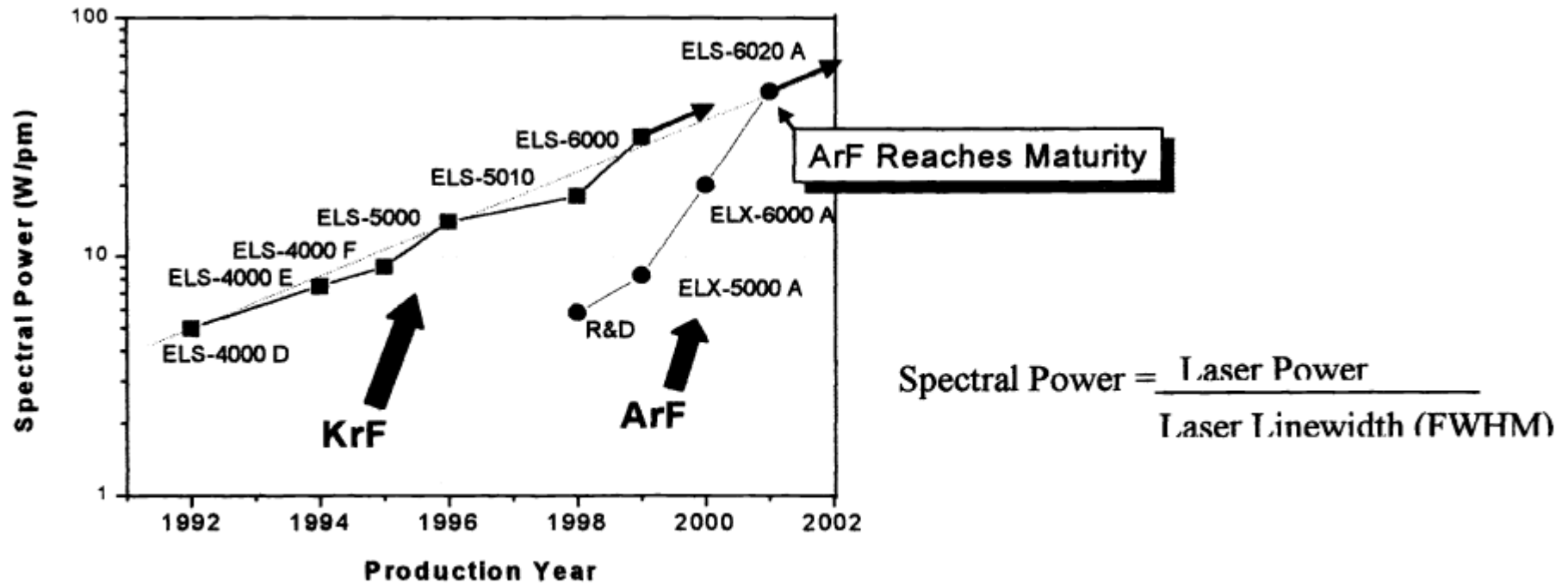
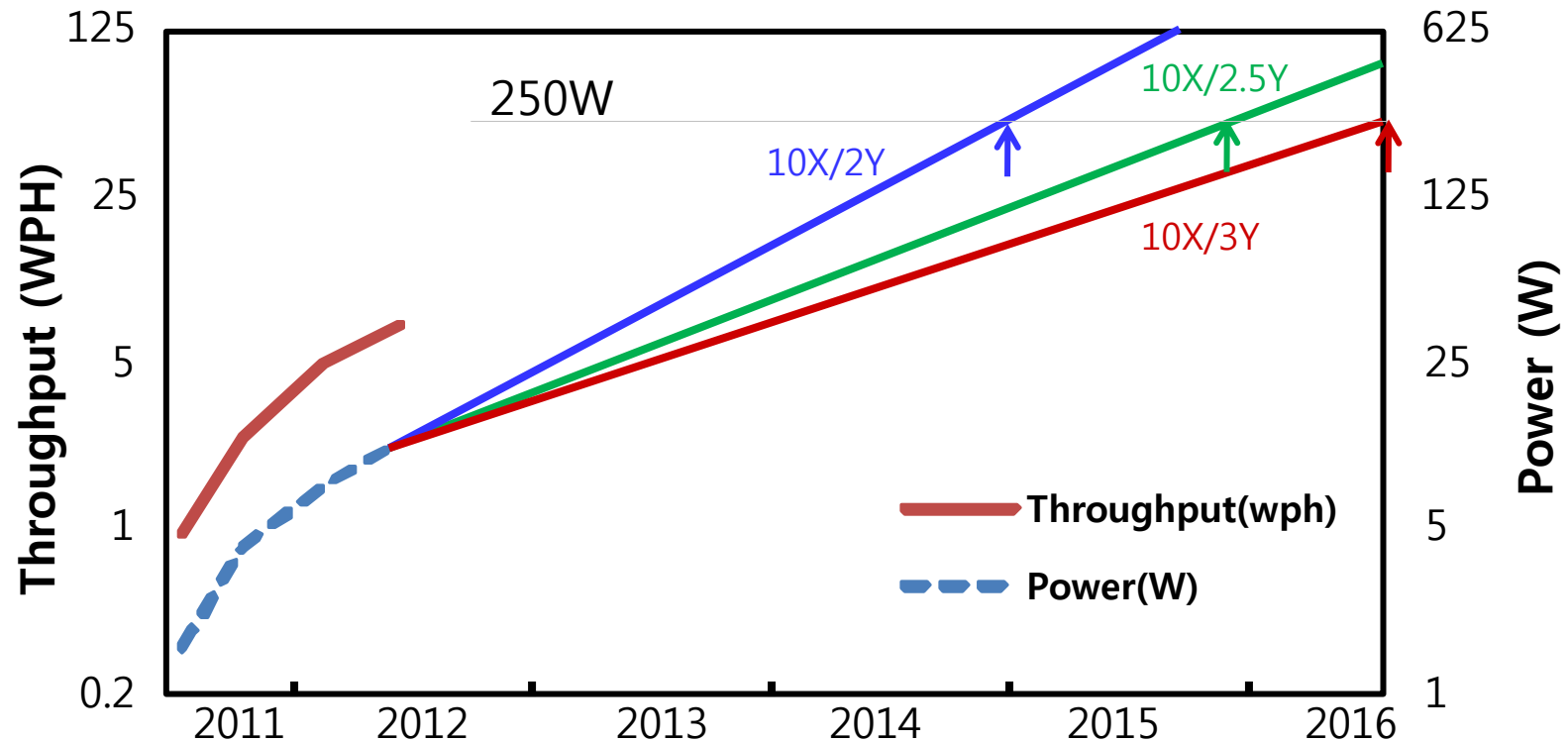


Figure 1: Historical trend of the Spectral Power.

10X power up for 9 years in 248nm, for 2.6 years in 193nm  
How long for 25X gap in 13.5nm?

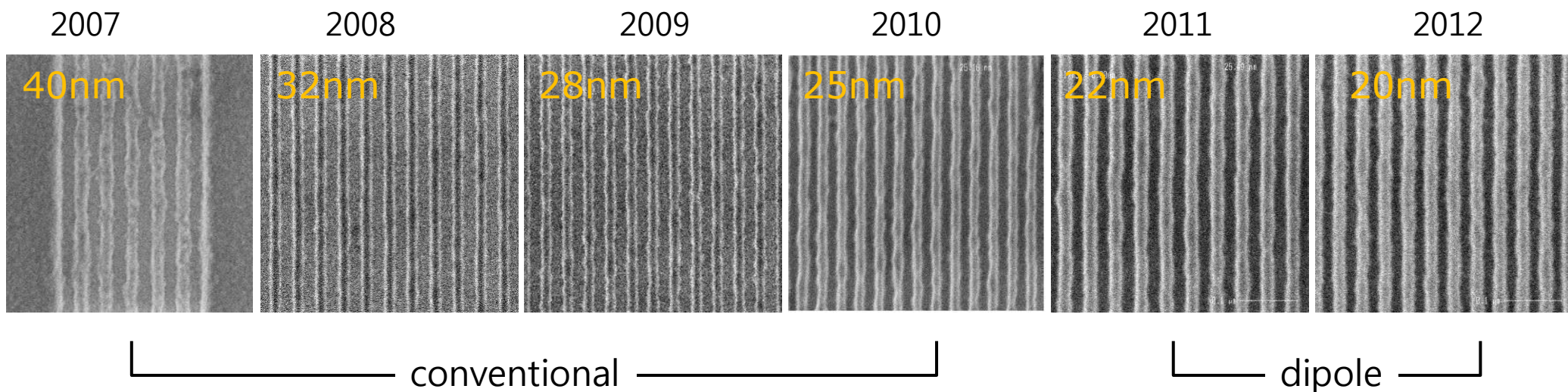
# Source prediction



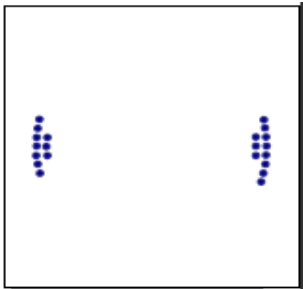
Improvement in next year very crucial, will decide the future

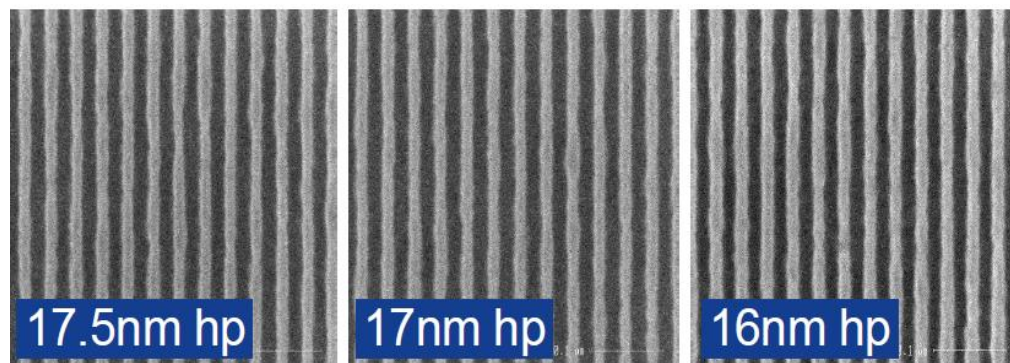
# Progress continues in resolution

## □ Yearly progress of EUV resolution performance



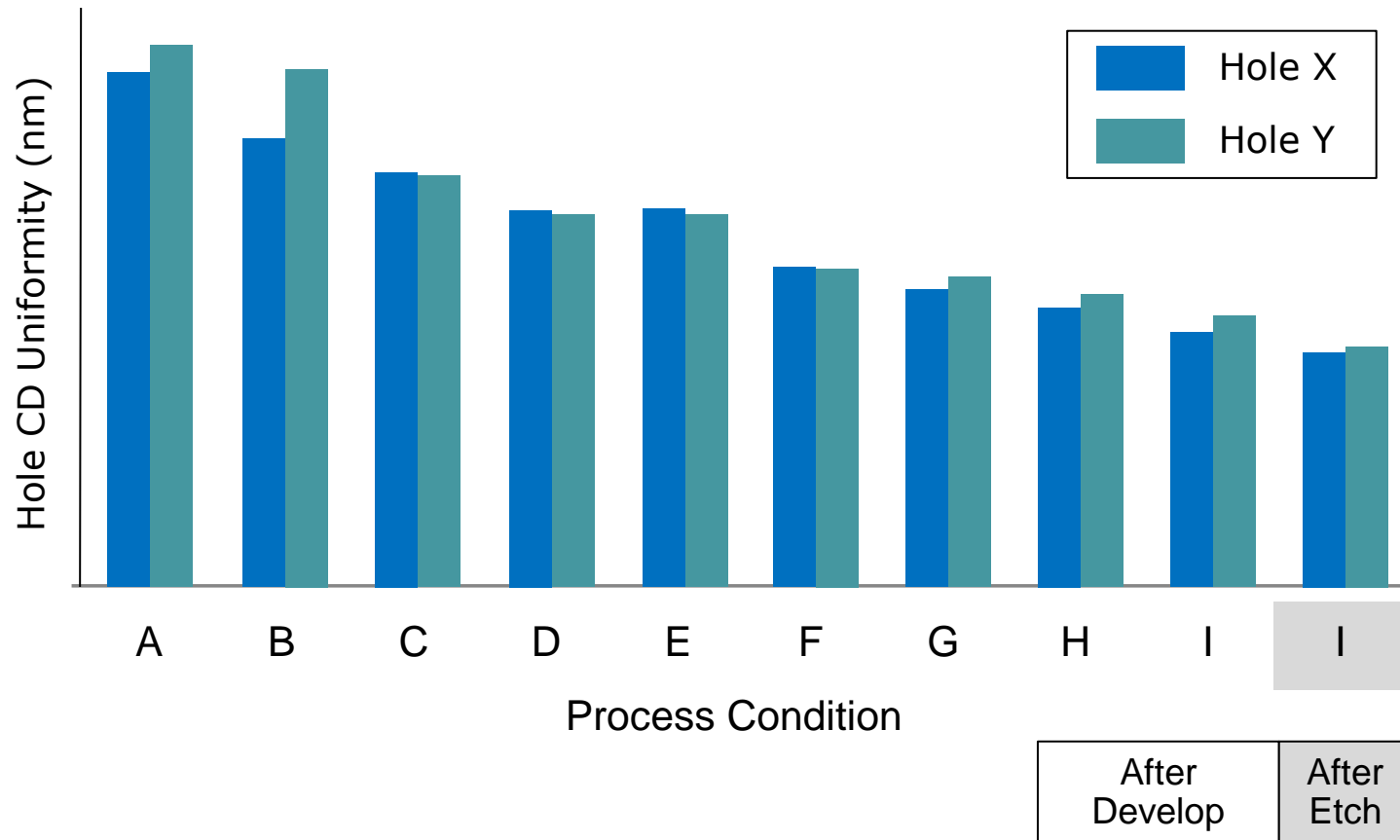
## ❖ Strong dipole @IMEC

  
✧ T. Wallow(GF) SPIE 2012



# Improvement in CDU of contact hole

□ total CDU progress

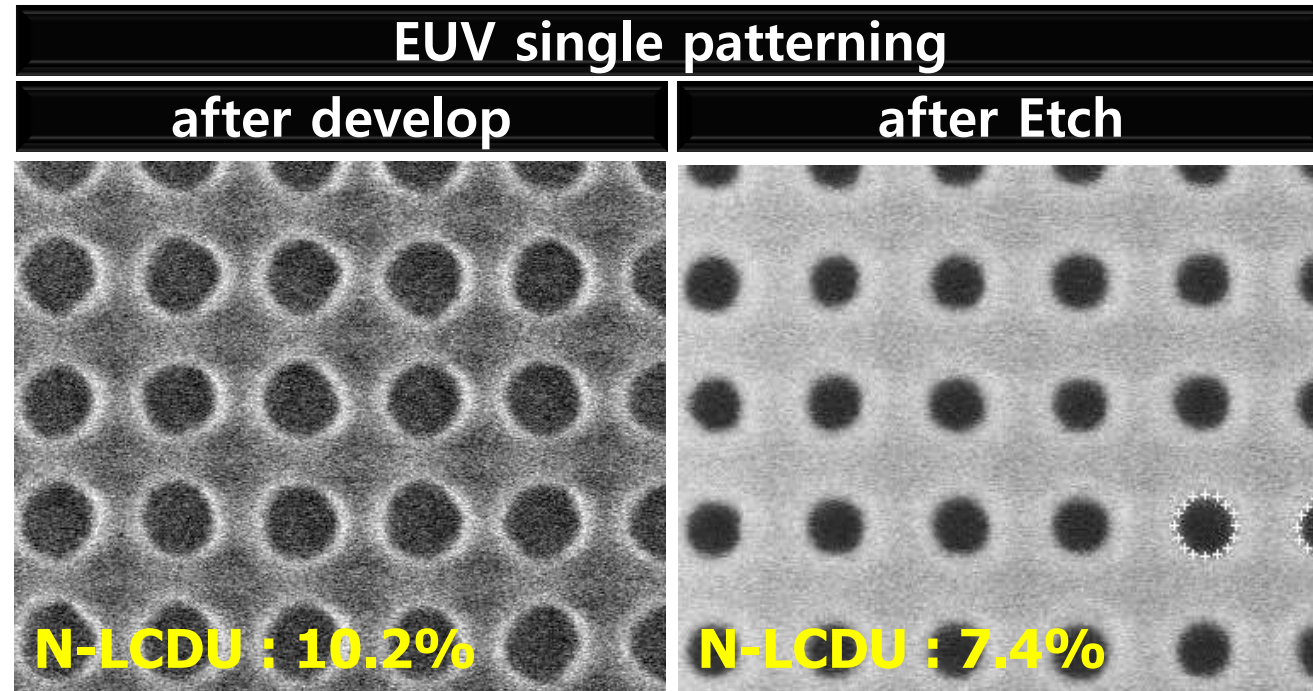
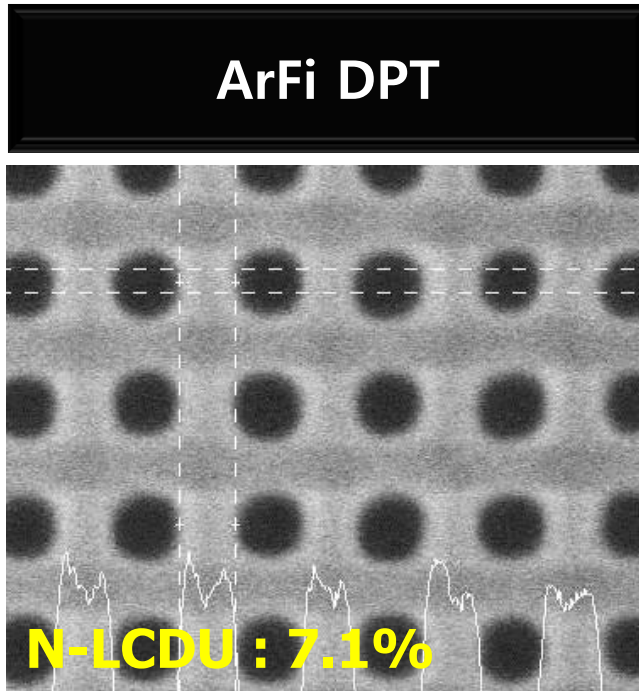


**EUVL CD uniformity has improved significantly through various process optimization of resist, mask, and illumination modes**

# Comparison ArFi Hole DPT vs. EUV

□ Normalized Local CDU, 193nm DP vs. EUV

※ K. Ban(SK hynix) SPIE 2012

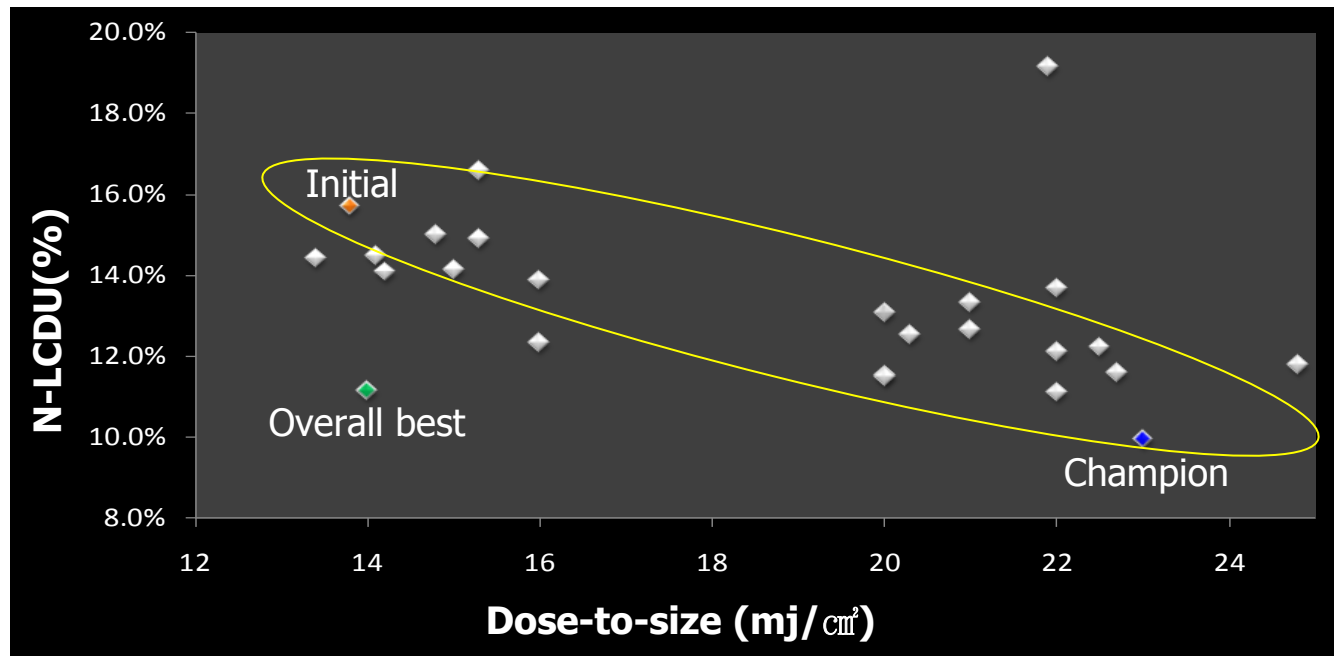


Regarding C/H CD uniformity, EUV lithography is comparable with ArFi DPT

# Resist Screening: Local CD variation

- ❑ High sensitive with better performed resist is essential

※ K. Ban(SK hynix) SPIE 2012

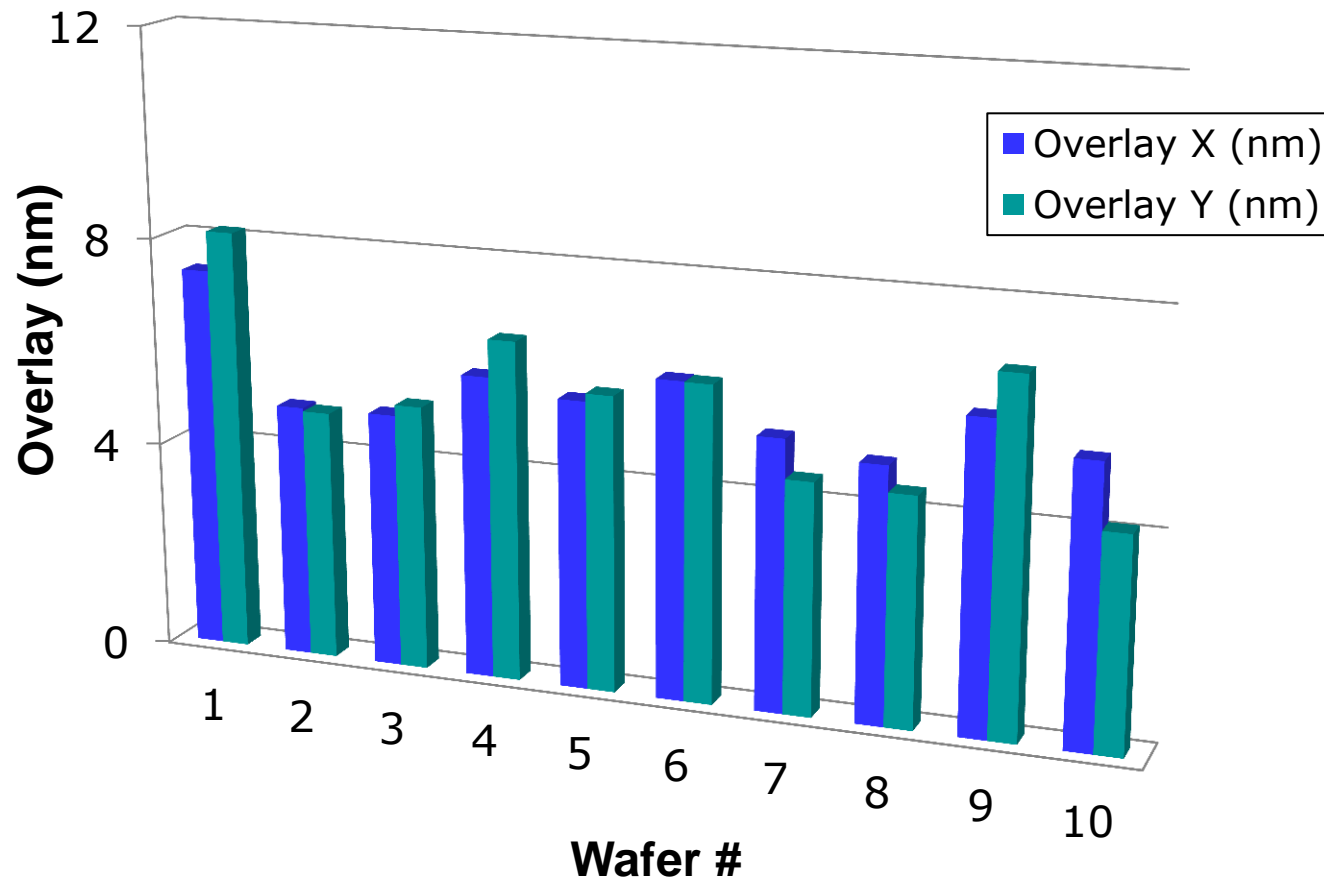


Dose sensitivity of resist more and more important as EUV source reveals difficulty in increasing power level

# On product overlay to ArF-i

※ B. Lee(SK hynix) EUVL Symposium 2011

## □ NXE3100 Matching overlay to NXT1950i



❖ Correction per exposure applied with linear alignment

# Intra-field overlay error

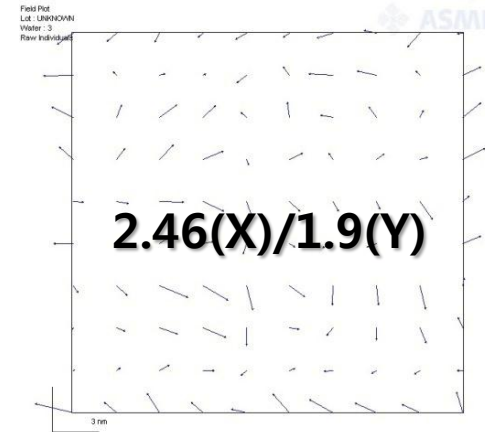
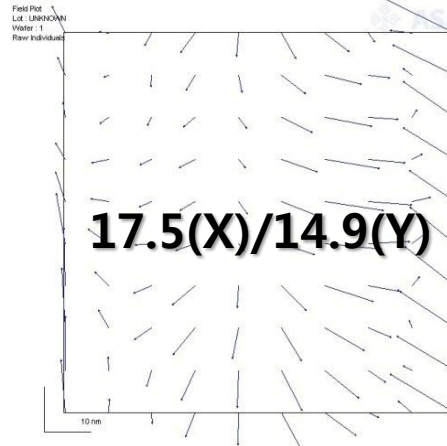
- measured with fully rotatable mask

※ B. Lee(SK hynix) EUVL Symposium 2011

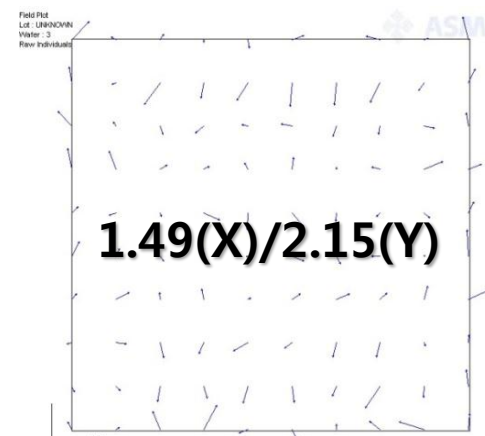
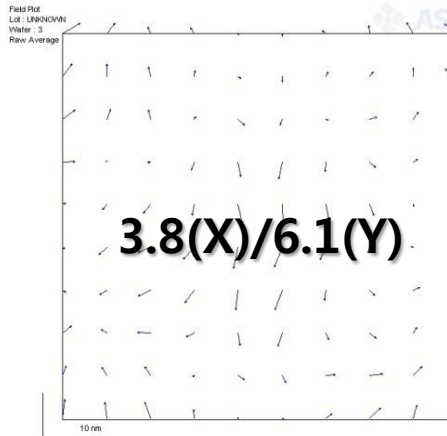
Field position dependent

Mask position dependent

Mask A  
@ ADT



Mask B  
@ PPT

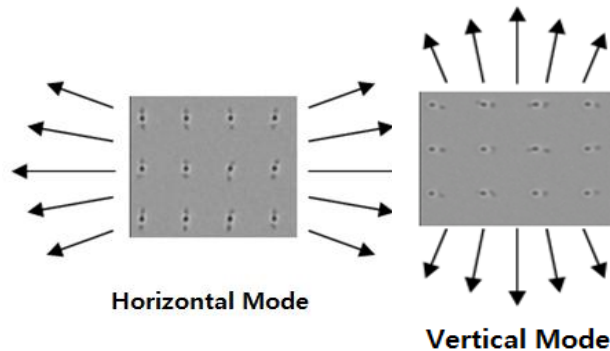
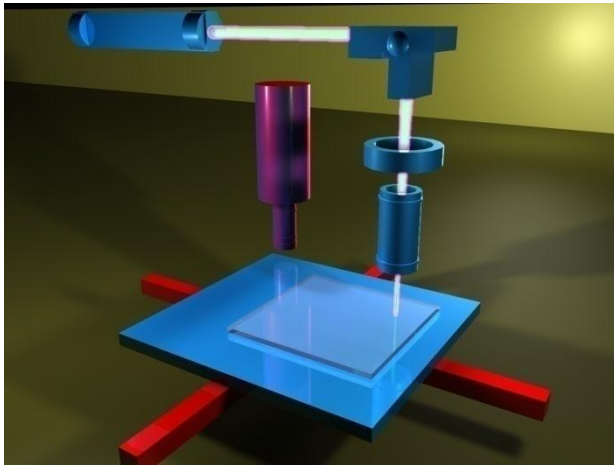


Early result promising, considering mask flatness effect of EUV

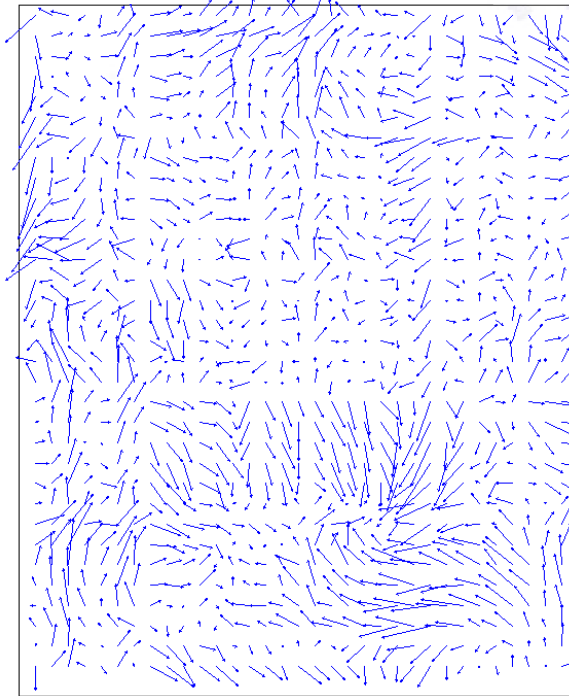
# Intra-field overlay after RegC®

- RegC applied to 193i mask only because of backside opacity of EUV mask

## Carl Zeiss' RegC®

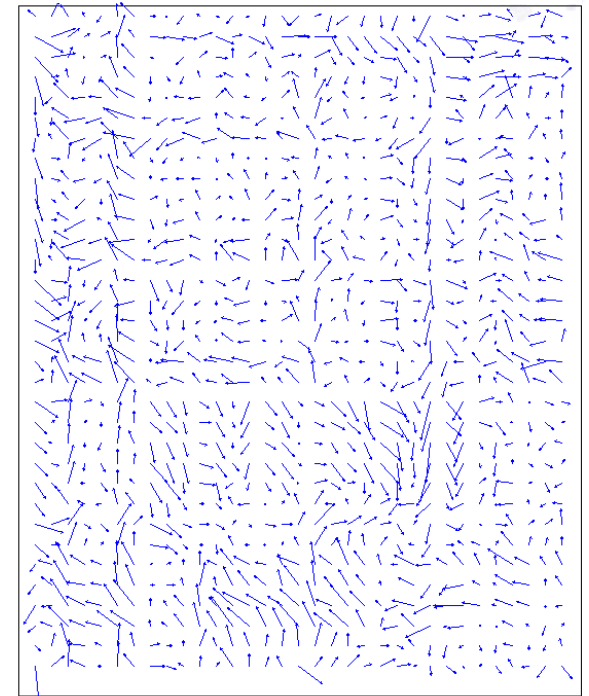


## Pre RegC®



4.74(X)/5.29(Y)

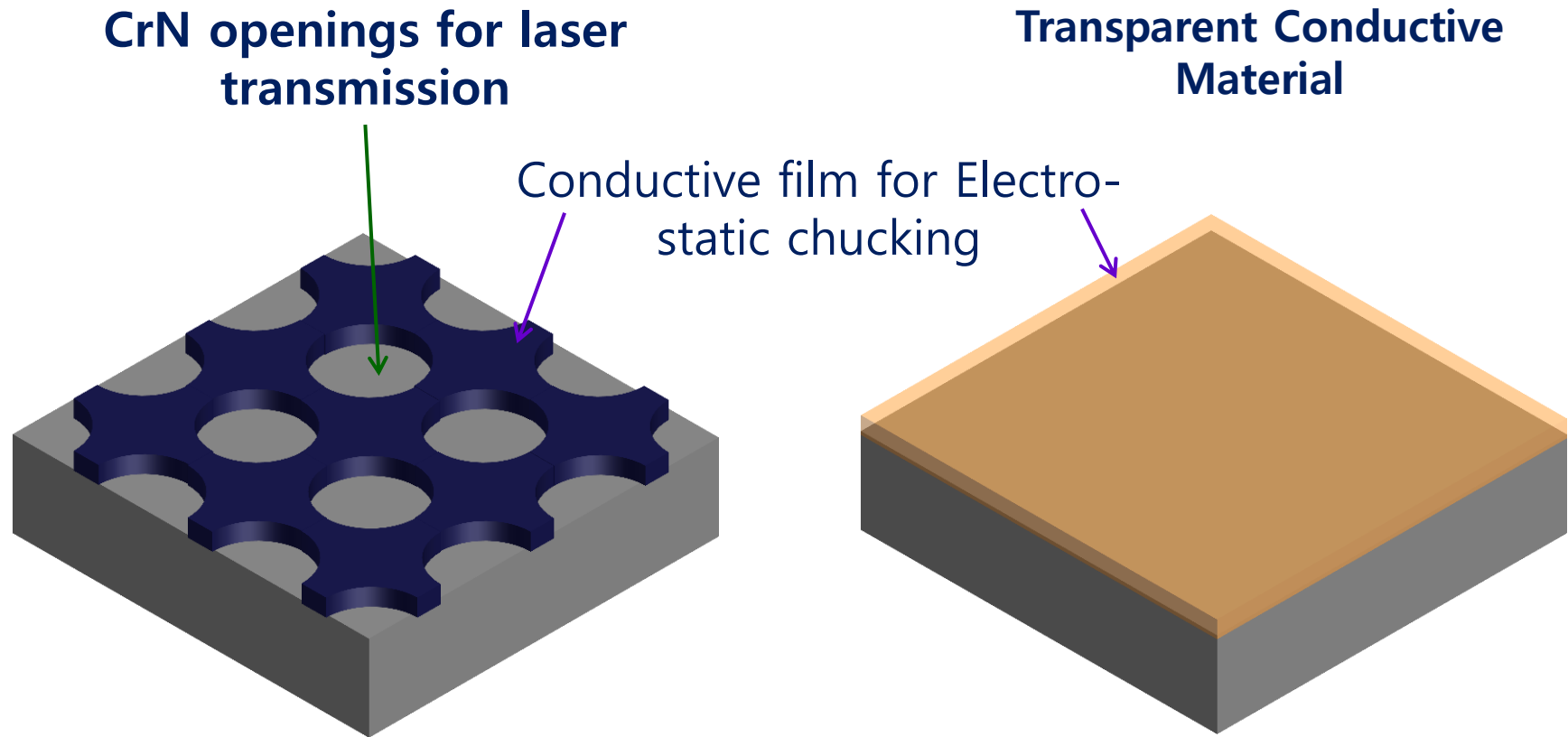
## Post RegC®



3.76(X)/4.18(Y)

**Intra-field term improvement 20%**

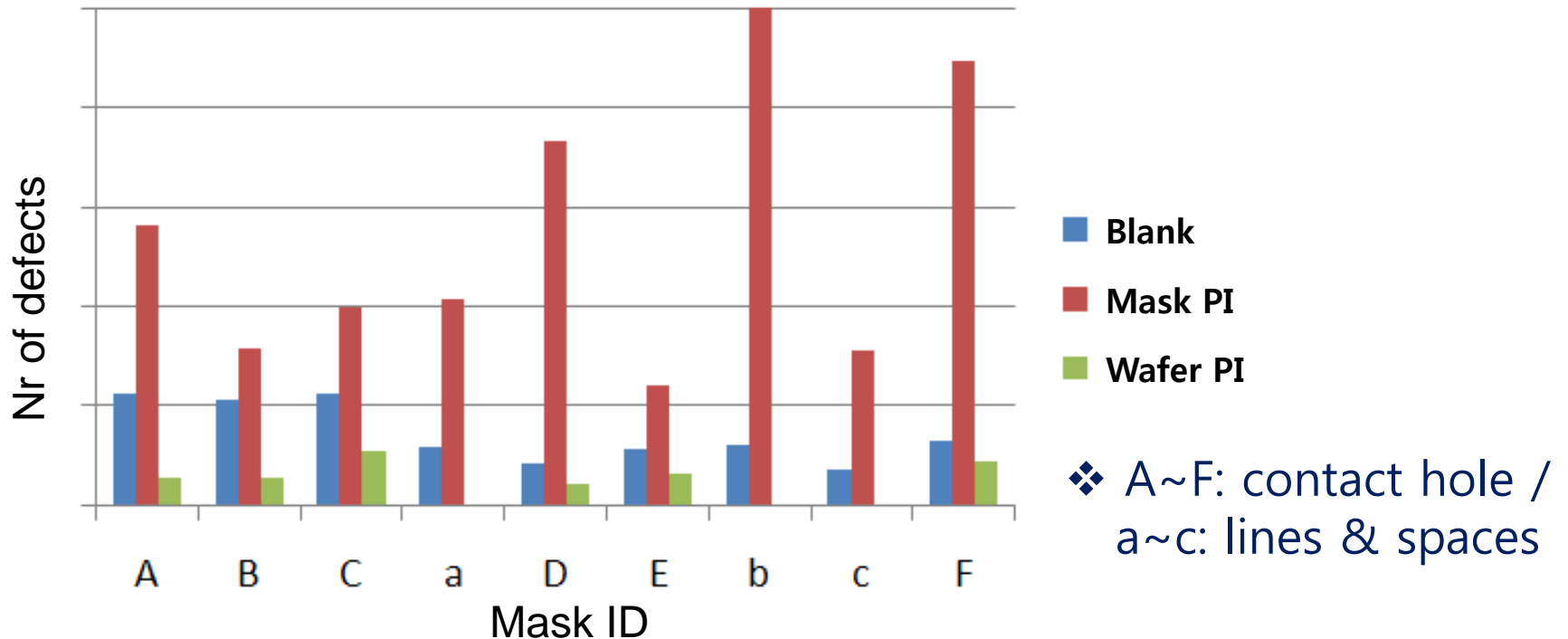
# EUV backside change required for RegC®



**Backside of EUV mask blank need to be changed for RegC application**

# Mask defect statistics

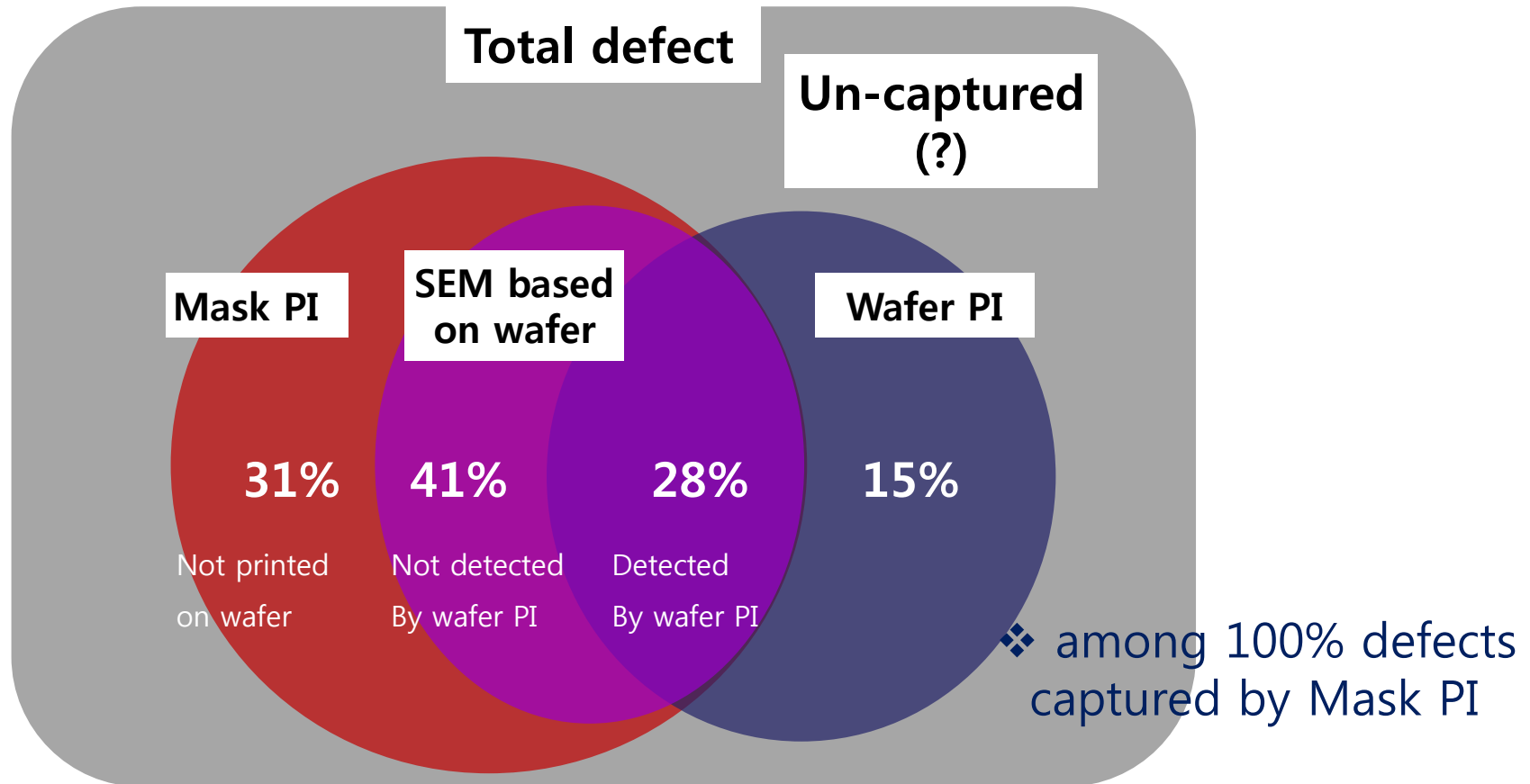
## ❑ Defect counts with different inspection tools



**No strong correlation between blank/ mask pattern/  
wafer pattern defects**

# Mask defect status quo

## ❑ Defect capture-ability of different inspection methods



**Make wafer PI capture all defects recognized by SEM!**

# Mask operation; EUV vs. DUV

## EUV



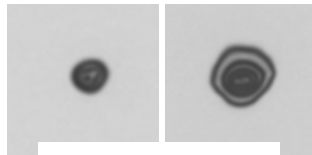
Dual PODs,  
pods exchanger



Inner POD(EIP)



Particle adder  
Thermal deformation(?)  
haze



Particle adder

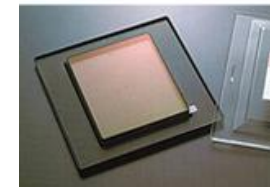
## DUV



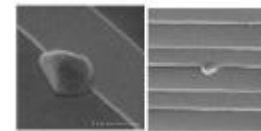
Shipping box



With pellicle



Particle growth  
(haze)



Proc. SPIE 83220S-2



# Mask operation; EUV vs. DUV

## EUV



Dual PODs,  
pods exchanger



Inner POD(EIP)



Particle adder  
Thermal deformation(?)  
haze



## Requirements

- Mask Transportation within dual pods

- Pellicle if possible

- **Keep Inner pods clean**  
(inner pods inspection method)

- **No adder during exposure**

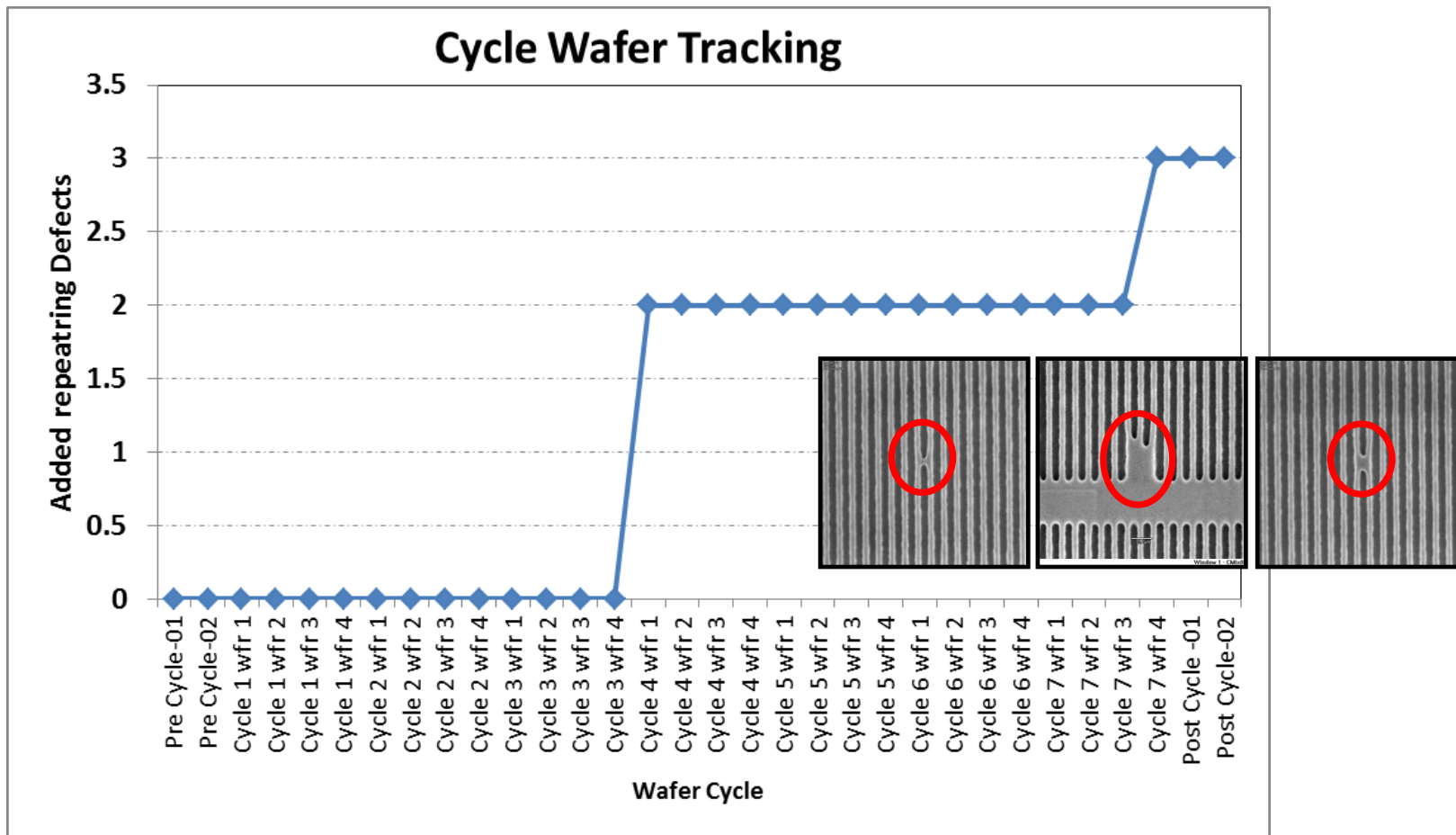
- Inspection of mask defect on wafer

- Mask cleaning at proper time

# Particle adder by wafer inspection

## □ i-PRP results

※ Y. Hyun(SK hynix) et. al. Poster session EUVL 2012



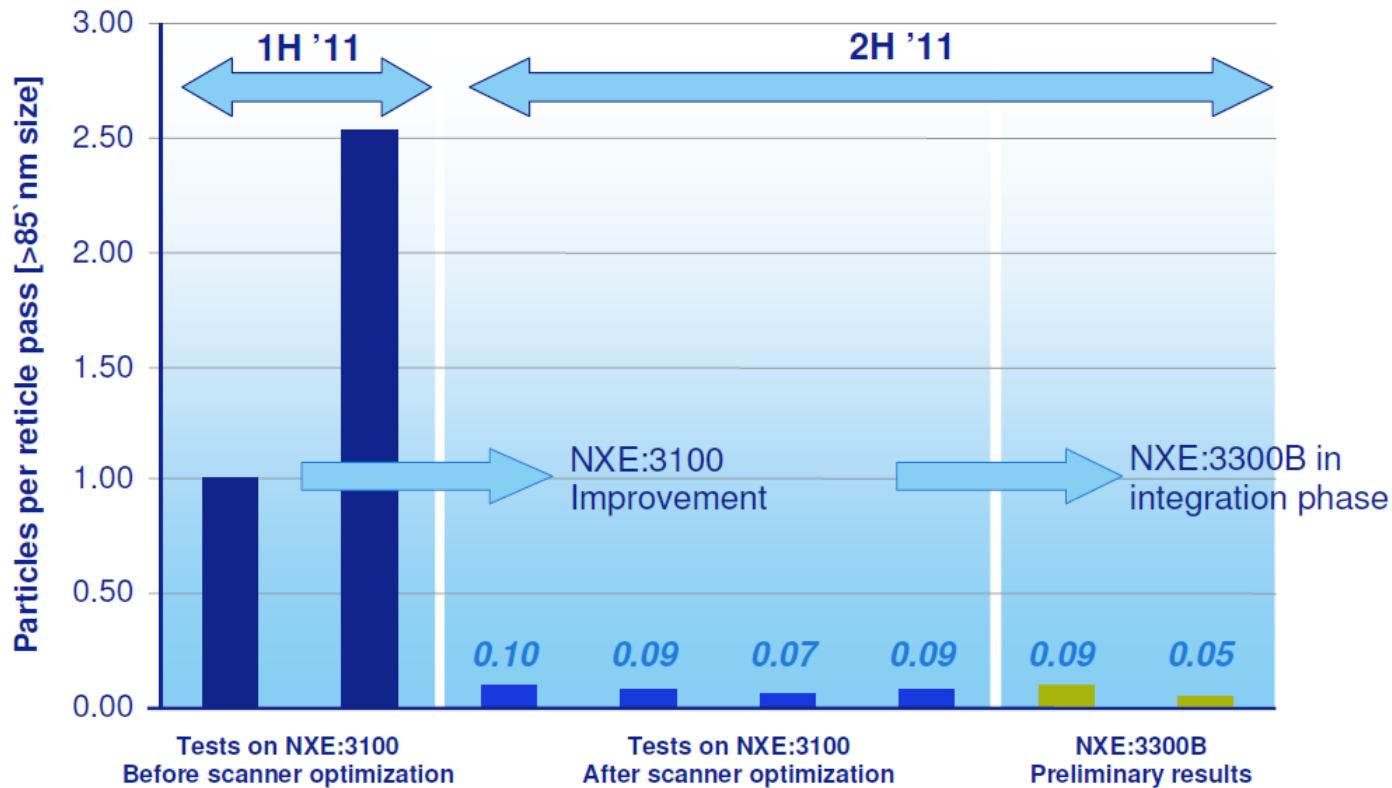
3 adders during 7 batches for 10 days confirmed

# Particle adder per pass on mask

※ Hans Meiling(ASML) SPIE 2012

## NXE reticle defect adders performance is improving

Target: <0.01 Particles-per-reticle-pass (PRP)

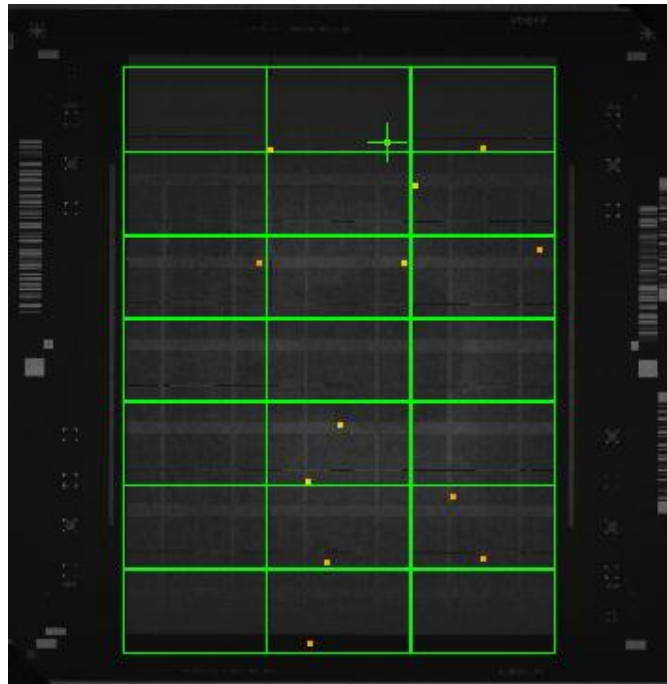
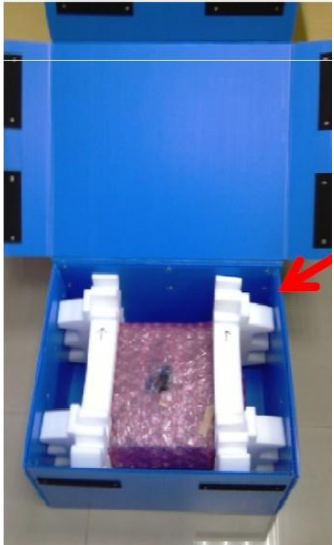


At least, added particles should be zero during exposure

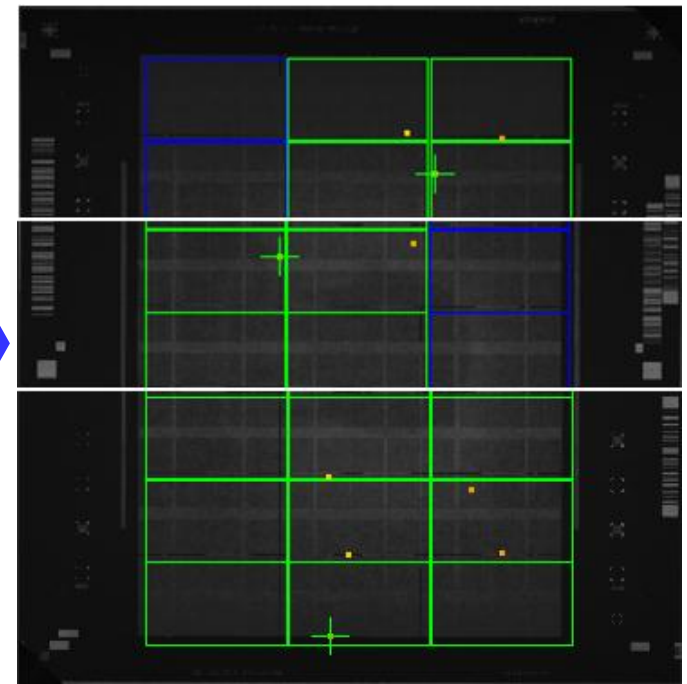
# Mask transport within dual pods

- ❑ Ground transportation of 80km distance in 5 cycles of round trip

Pre inspection



Final inspection



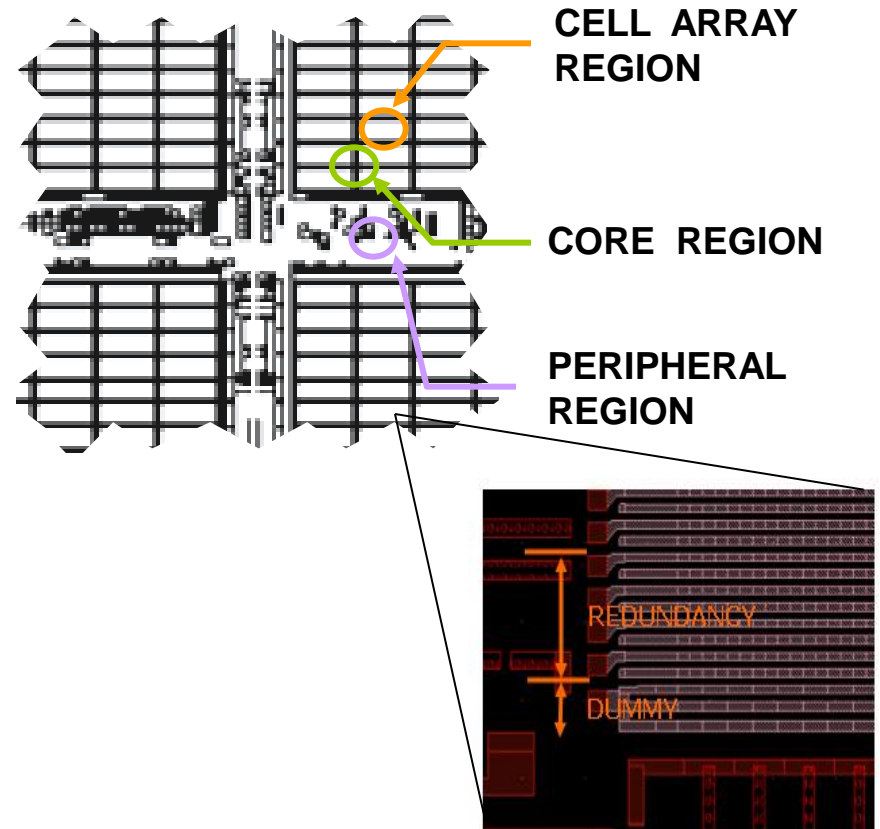
No adder found on mask!

Test done on Gudeng, Entegris pods test will follow

# Mask defects on memory

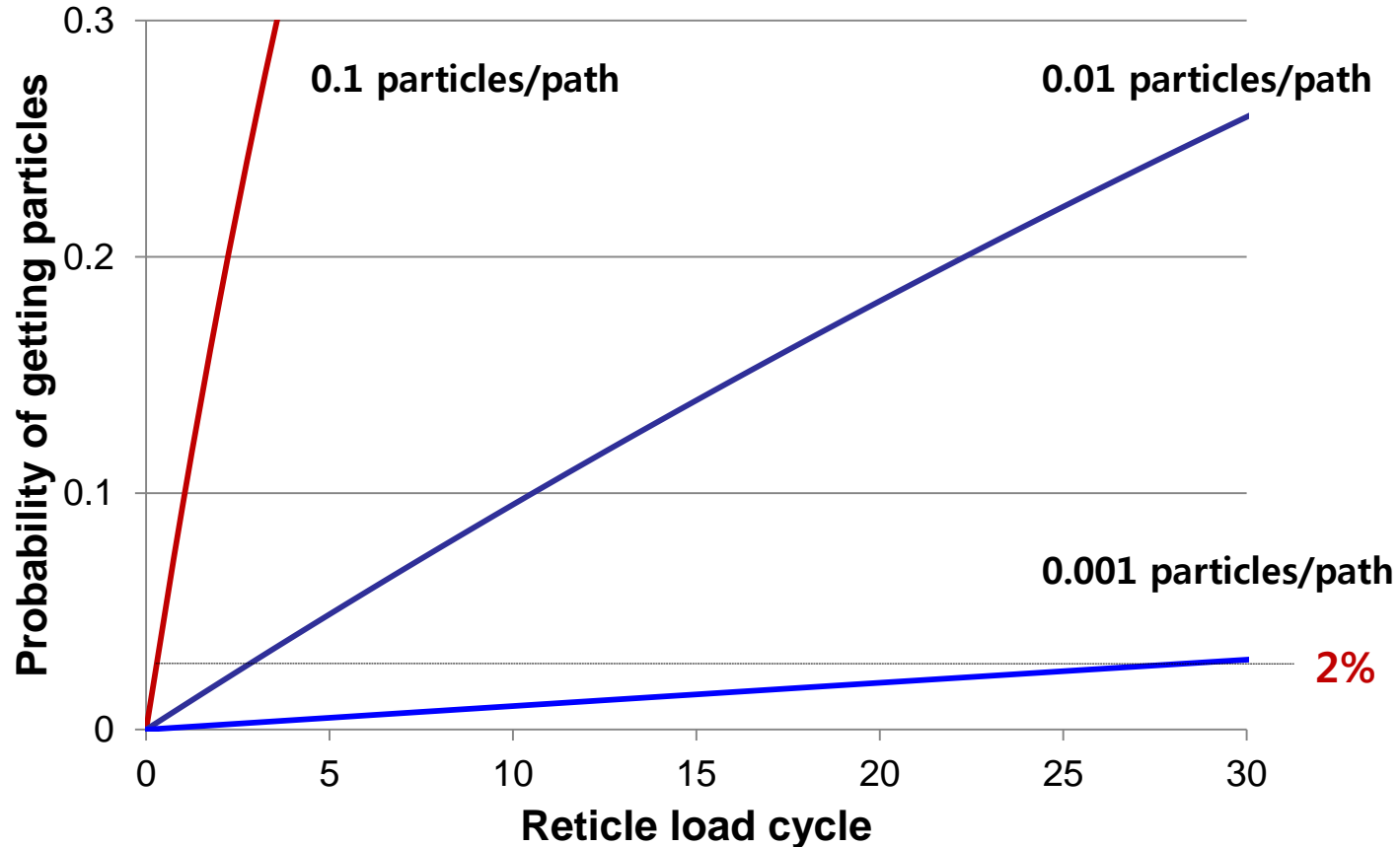
## □ memory IC truth

1. 10~20 dies within a mask (chip size small)
2. **Redundancy** included
3. Defect in Cell/Core area **can be repaired (not always)**
4. Killer defect in **peripheral circuit area** with relatively **low printability** because of relaxed design rule



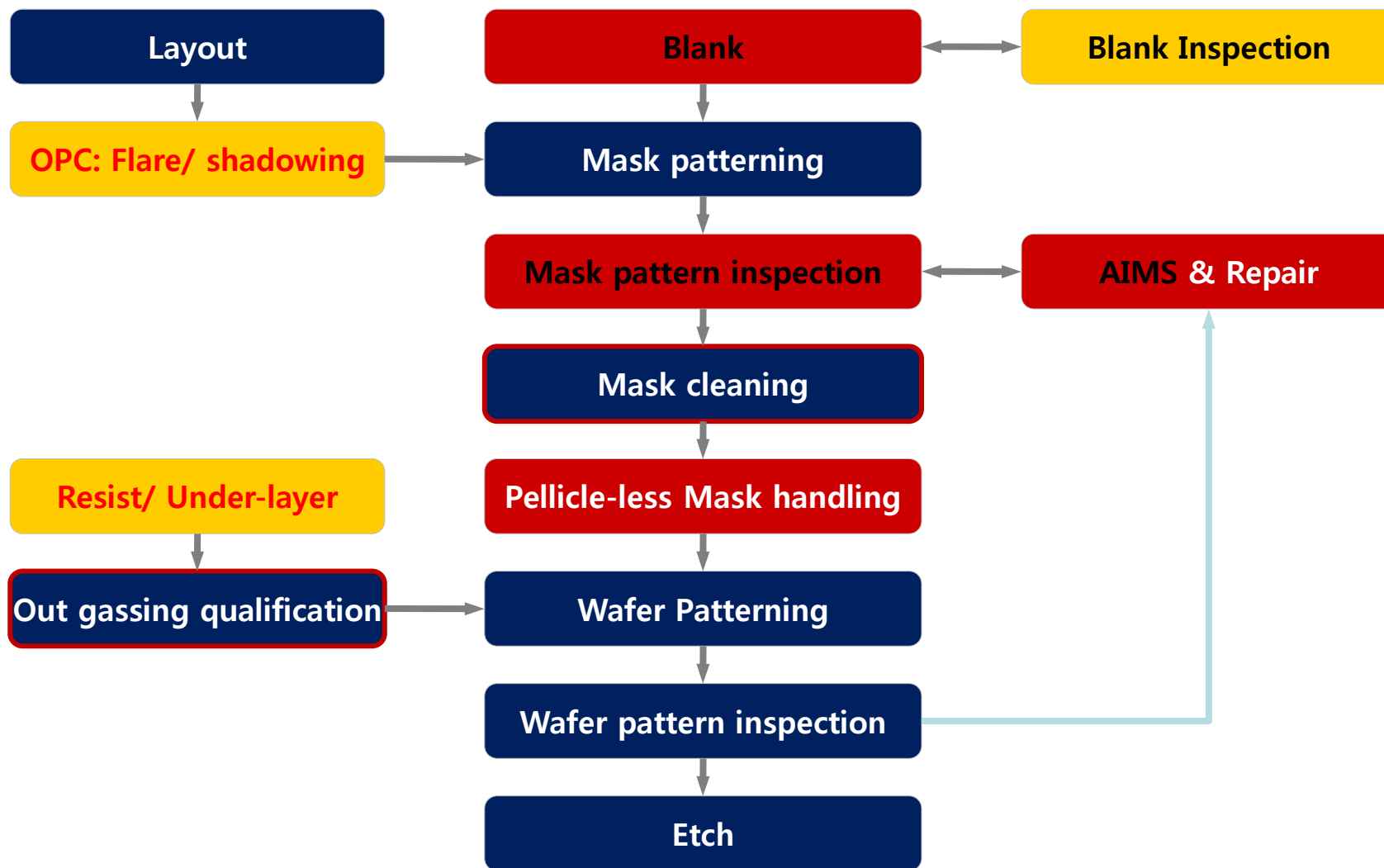
# How many particles?

## □ probability of particle on mask



- ✓ If 2% rework rate assumed as a guide-line, mask cleaning should be after every 2 batches @0.01 PRP
- ✓ Particle adder can be more than a increasing rework rate?

# EUV readiness in overall flow



# Closing; distant and close view

※ *Sun Jung, Korean landscape painting master(1676~1759)*



Mountain looks very steep and un-challengeable at far sight,  
but there always passages to climb over as we get close

# Thank You...

